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ENERGY EFFICIENT MULTIPLIER WITH ADAPTIVE HOLD LOGIC

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ABSTRACT

Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The throughput of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias, increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier.

INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating an integrated circuit(IC) by combining thousands of transistors into a single chip. Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. Digital multipliers are widely used in arithmetic units of microprocessors, multimedia and digital signal processors. The redundant binary number representation has been introduced by Avizienis to perform signed-digit arithmetic; the RB number has the capability to be represented in different ways. Fast multipliers can be designed using redundant binary addition trees. The redundant binary representation has also been applied to a floating-point processor and implemented in VLSI. High performance RB multipliers have become popular due to the advantageous features, such as high modularity and carry-free addition .A RB multiplier consists of a RB partial product (RBPP) generator, a RBPP reduction tree and a RB-NB converter.

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EXISTING SYSTEM

The aging of the sleep transistor is evaluated in terms of current capability degradation. The latter is then used in the second phase to estimate the delay degradation of the power-gated logic circuit.

- Sleep-Transistor Current Capability Degradation: This analysis consists of a two-step simulation: the prestress simulation phase, in which we estimate the aging effects on the pMOS sleep transistor, and the poststress simulation phase, in which the stress information is integrated into the pMOS device parameters. According to the properties of the sleep signal (defined by its zero static probability and voltage level), and the user-defined environmental setup (V_{dd} voltage, virtual-V_{dd} voltage, temperature, BB V_{bs}, and temperature), the prestress simulation computes the aging of the pMOS sleep transistor after a userdefined usage time. The amount of aging, calculated on the base of the builtin aging models integrated into Synopsys HSPICE and the technology parameters provided by the silicon vendor, is then translated and annotated into device parameter degradation, i.e., threshold voltage degradation (i.e., ΔV_{th}). As shown in Fig. 3.1, during poststress simulation, the NBTI-induced V_{th} degradation is modeled using a voltage source on the gate terminal of the sleep transistor. At the end of the pre- and poststress simulations, we have a complete characterization of the current drive profile before and after NBTI stress. In other words, we are able to estimate the degradation over time of the maximum current drained by the pMOS sleep transistor ($\Delta I_{ds} = I_{ds}' - I_{ds}$), for a given value of usage time and for any operating condition.

  Since NBTI effects on sleep transistors induce performance slowdown throughout the lifetime of the circuit, it is important to identify a set of effective low-cost NBTI-tolerant implementations of power gating. In the sequel, we present some possible solutions, in which aging is controlled by means of three basic strategies, i.e., transistor OS, BB, and control of equivalent stress probability. Each technique results into some area and leakage overheads; thus, it is possible to combine them into hybrid solutions, which can achieve better tradeoffs between leakage and aging. We will first outline the basic features of the three strategies and eventually describe their possible variants.

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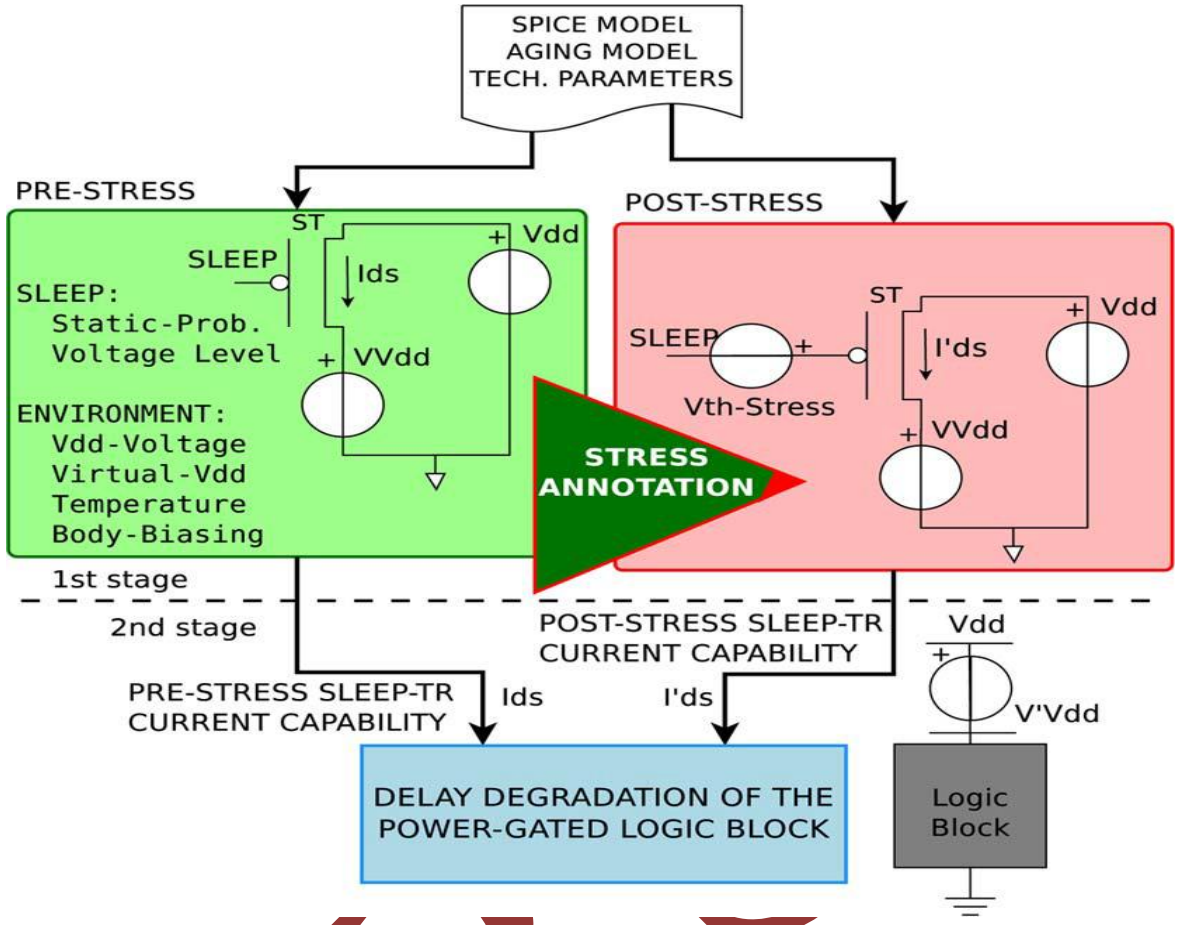

Fig. 1. NBTI-characterization flow for pMOS sleep transistor

PROPOSED SYSTEM

The NBTI (PBTI) effect occurs when a pMOS (nMOS) transistor is under negative (positive) bias voltage, resulting in Vth drift. When the bias voltage is removed, the recovery process occurs, reducing the Vth drift. If a pMOS (nMOS) transistor is under constant stress, this is referred to as static NBTI (PBTI). If both stress and recovery phases exist, it is referred to as dynamic NBTI (PBTI). The Vth drift of pMOS (nMOS) transistor due to the static NBTI (PBTI) effect can be described by dc reaction-diffusion (RD) framework. If transistors are under alternative stress and recovery phases, the dc RD model should be modified to an ac RD model

$$\Delta V_{th}(t) \cong K_{AC} \times t^n \cong \alpha(S, f) \times K_{DC} \times t^n \quad (4.1)$$

where α is a function of stress frequency (f) and signal probability (S). Since the impact of frequency is relatively insignificant, the effect of signal frequency is ignored. K_{DC} is a technology-dependent constant

$$K_{DC} = A \times T_{OX} \times \sqrt{C_{OX}(V_{GS} - V_{th})} \times [1 - V_{DS}/\alpha(V_{GS} - V_{th})] \times \exp(E_{OX}/E_0) \times \exp(-E_a/kT) \quad (4.2)$$

where A is a constant, and T_{OX} is the oxide thickness. E_{OX} is the gate electric field, which is $(V_{GS}–V_{th})/T_{OX}$; k is the Boltzmann constant, and T is the temperature. E_0 and E_a are

technology-independent characteristics of the reaction that are equal to 1.9–2.0 MV/cm and 0.12 eV, respectively.

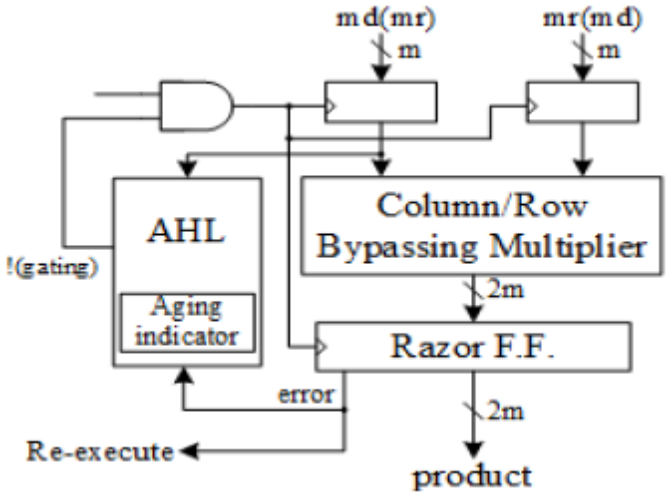

Fig. 2. Proposed architecture (md means multiplicand; mr means multiplicator).

Fig. 2 shows our proposed aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops and an AHL circuit. The inputs of the row-bypassing multiplier are the symbols in the parentheses. In the proposed architecture, the column- and row-bypassing multipliers can be examined by the number of zeros in either the multiplicand or multiplicator to predict whether the operation requires one cycle or two cycles to complete. When input patterns are random, the number of zeros and ones in the multiplicator and multiplicand follows a normal distribution. Therefore, using the number of zeros or ones as the judging criteria results in similar outcomes. Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives. Fig. 4.6 shows the details of Razor flip-flops. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result.

If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to reexecute the operation and notify the AHL circuit that an error has occurred. We use Razor flip-flops to detect whether an operation that is considered to be a one-cycle pattern can really finish in a cycle. If not, the operation is reexecuted with two cycles. Although the reexecution may seem costly, the overall cost is low because the reexecution frequency is low. More details for the Razor flip-flop can be found. The AHL circuit is the key component in the aging-ware variable-latency multiplier.

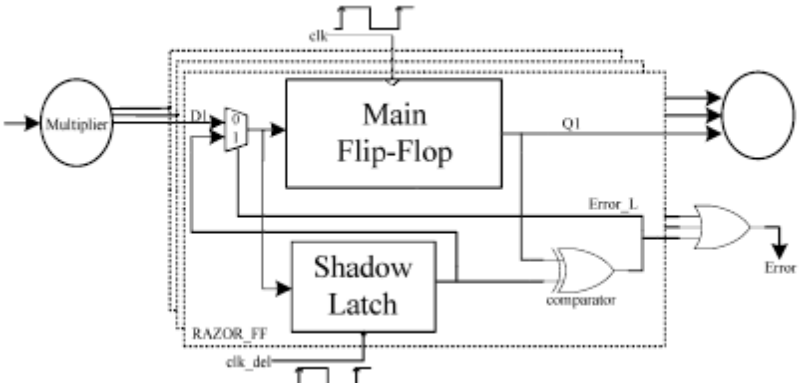

Fig. 3. Razor flip flops

In summary, our proposed multiplier design has three key features. First, it is a variable-latency design that minimizes the timing waste of the noncritical paths. Second, it can provide reliable operations even after the aging effect occurs. The Razor flip-flops detect the timing violations and reexecute the operations using two cycles. Finally, our architecture can adjust the percentage of one-cycle patterns to minimize performance degradation due to the aging effect. When the circuit is aged, and many errors occur, the AHL circuit uses the second judging block to decide if an input is one cycle or two cycles.

RESULTS AND DISCUSSION

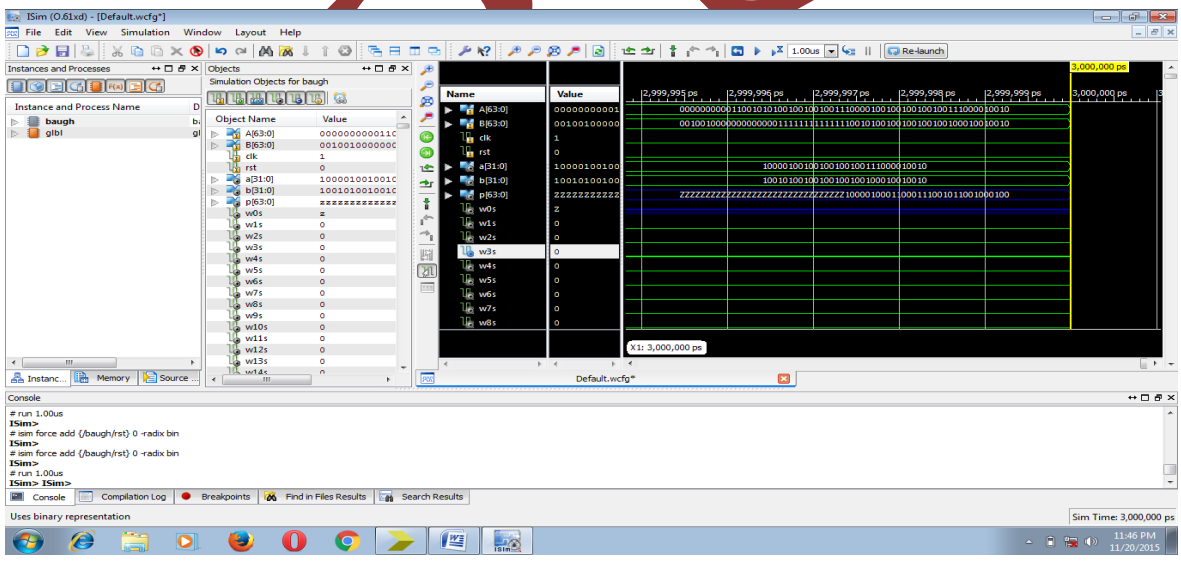

Fig.4.Output Waveform

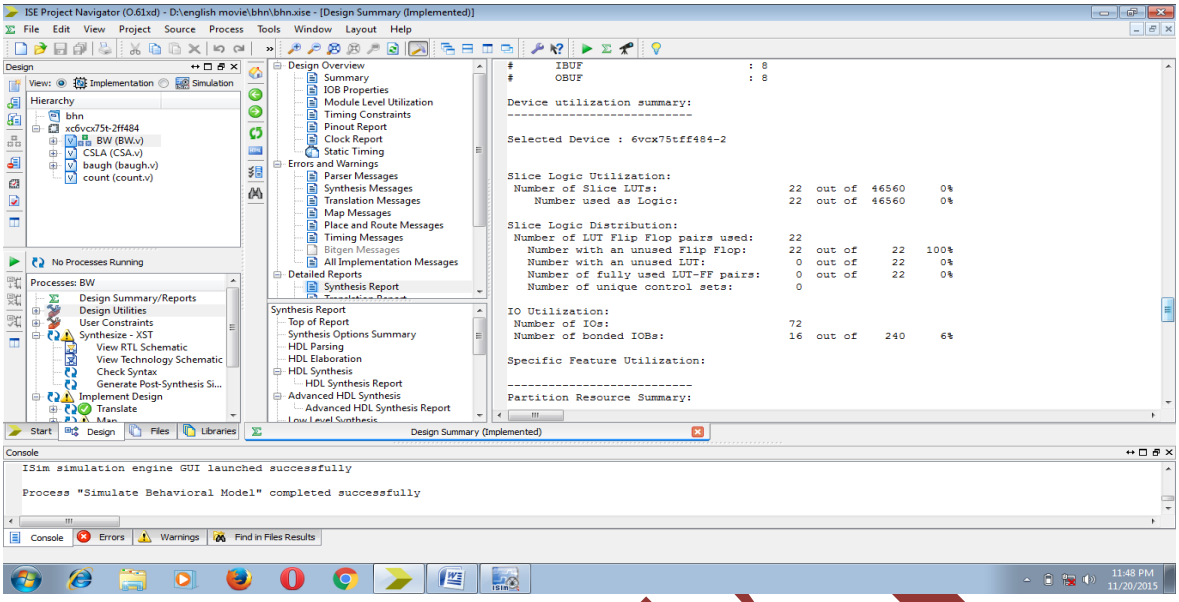

Fig.5.Output of Area Analysis

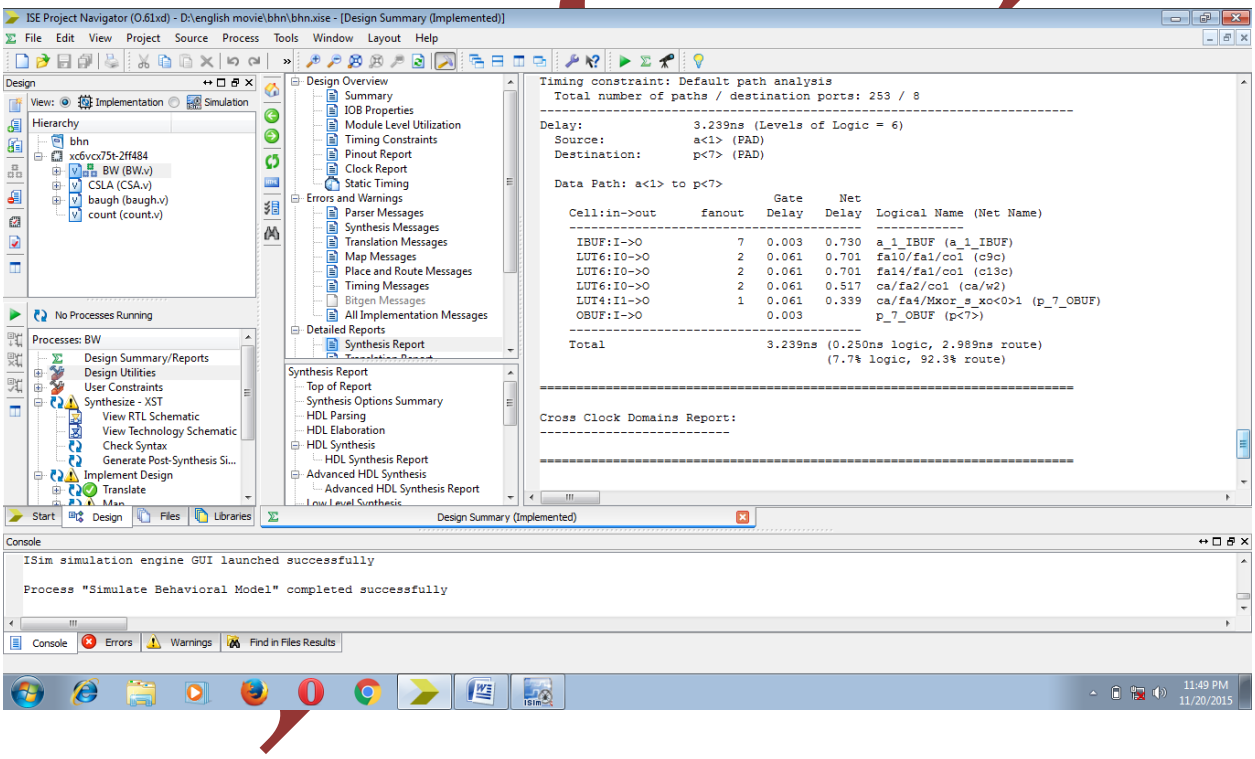

Fig.6.Output of Delay Analysis

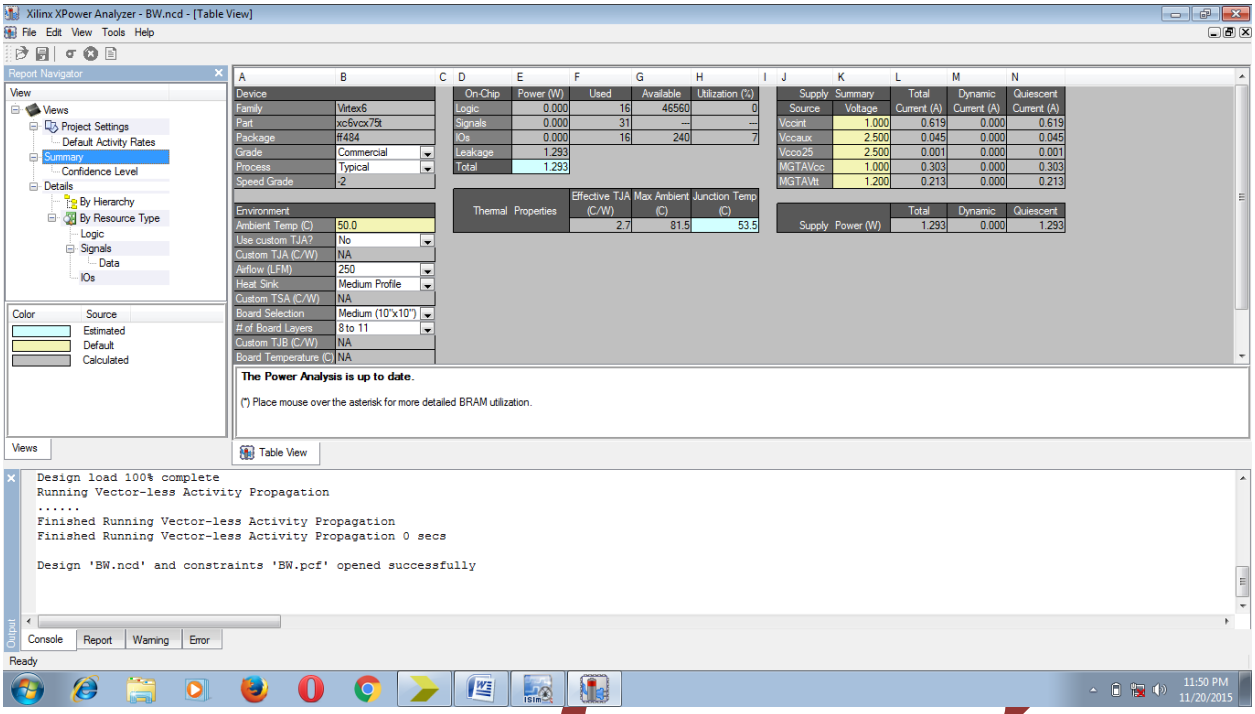

Fig.7.Output of Power Analysis

CONCLUSION

This project proposes an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. In addition, the variable-latency bypassing multipliers exhibited the lowest average EDP and achieved up to 10.45% EDP reduction in 32 × 32 VLCB multipliers. Electromigration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow. The metal atoms will be gradually displaced after a period of time, and the geometry of the wires will change. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, electromigration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences. If the aging effects caused by the BTI effect and electromigration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electromigration. In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electromigration and use the worst case delay as the cycle period.

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