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FINFET VS 32NM CONVENTIONAL MOSFET USING DEVICE SIMULATION

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ABSTRACT

FinFET devices used to replace conventional MOSFET with decrease in threshold voltage hence reduced the power consumption. SOI technology used for the devices i.e. FinFET. We provide a comparison of 32nm FinFET with conventional MOSFET. 32nm FinFET based on SOI gives better output results i.e. reduced threshold voltage, controlling leakage, minimize short channel effect over 32nm conventional MOSFET. To overcome the short channel effect, a suitable threshold voltage is required with the scaling trend in device dimension. Independent gating of the finFET's double gate provides reduction in leakage current.

INTRODUCTION

The basic principle of transistor was first patented by Julius Edgar Lilienfeld in 1925. 25 years later, when Bell Telephone attempted to patent the junction transistor, they found Lilienfeld already holding a patent, worded in a way that would include all types of transistors. Bell Labs was able to work out an agreement with Lilienfeld. It was at that time the Bell Labs version was given the name bipolar junction transistor, or simply junction transistor, and Lilienfeld's design took the name field effect transistor. In 1959 M. M. (John) Atalla and Dawon Kahng at Bell Labs find the first successful insulated-gate field-effect transistor (FET), which had been long anticipated by Lilienfeld, Heil, Shockley and others. Operationally and structurally different from the bipolar junction transistor (BJT), the MOSFET was made by putting an insulating layer on the surface of the semiconductor and then placing a metallic gate electrode on that. It used crystalline silicon for the semiconductor and a thermally oxidized layer of silicon dioxide for the insulator. The silicon MOSFET did not generate localized electron traps at the interface between the silicon and its native oxide layer, and thus was inherently free from the trapping and scattering of carriers that had impeded the performance of earlier field-effect transistors.

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Following the development of clean rooms to reduce contamination to levels never before thought necessary, and of photolithography and the planar process to allow circuits to be made in very few steps, the Si–SiO2 system possessed such technical attractions as low cost of production (on a per circuit basis) and ease of integration. Largely because of these two factors, the MOSFET has become the most widely used type of transistor in integrated circuits. Additionally, the method of coupling two complementary MOSFETS (P-channel and N-channel) into one high/low switch, known as CMOS, means that digital circuits dissipate very little power except when actually switched. Some of the new technologies are Silicon on Insulator (SOI), Strained Silicon (S-Si) at the channel, inclusion of high-k dielectric materials in gate oxide and Multi gate MOSFETs. Many of these devices have been shown to have favourable device properties and new device characteristics, and require new fabrication techniques. These nanoscale devices have a significant potential to revolutionize the fabrication and integration of electronic systems and scale beyond the perceived scaling limitations of traditional CMOS. The earliest microprocessors starting in 1970 were all "MOS microprocessors"—i.e., fabricated entirely from PMOS logic or fabricated entirely from NMOS logic. In the 1970s, "MOS microprocessors" were often contrasted with "CMOS microprocessors" and "bipolar bit-slice processors" [2].

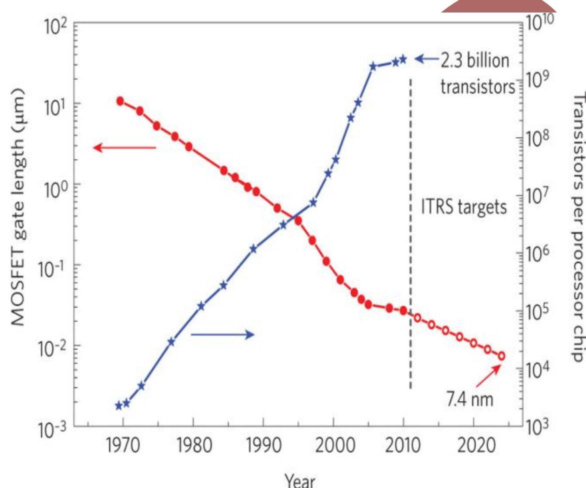

Figure 1 Decreasing Gate Length and increasing number of Transistors per chip [1].

The Scaling of MOSFET device to sub-40mn is very critical because of short channel effect (SCE). The SCE is mainly due to power supply since scaling of device is more rapid as compared to the scaling of supply voltage result is the SCE, because of high electric field degrades the mobility and causes velocity saturation. The gate loses control and short channel device is controlled by both gate and drain bias, the drain voltage gives more influence to the channel potential in nanoscale MOSFET. Device scaling has been a relatively straightforward

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affair thus far, but physical limits are fast being approached, and new materials and device structures are needed to continue scaling trends. The planar bulk-silicon MOSFET has been the workhorse of the semiconductor industry over the last 40 years. However, as the gate length is reduced, the capacitive coupling of the channel potential to the source and drain increases relative of the gate, leading to significantly degraded short-channel effects (SCE). This manifests itself as (a) increased off-stat leakage, (b) threshold voltage (V_{TH}) roll-off, i.e. smaller V_{TH} at shorter gate lengths, and (c) reduction of V_{TH} with increasing drain bias due to a modulation of the source-channel potential barrier by the drain voltage, also called drain-induced barrier lowering (DIBL).

PROPOSED METHODOLOGY

DEVEDIT is an interactive tool for structure and mesh specification and refinement. It is a device structure editor. It can be used to generate a new mesh on an existing structure and can be used to create or modify a device. These devices can then be used by 2D and 3D simulators. DEVEDIT can be used as a simulator used DECKBUILD or through a Graphical User Interface (GUI) [3].

ATLAS is very often used in conjunction with the ATHENA process simulator. ATHENA predicts the physical structures that result from processing steps. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions [6]. ATLAS is normally used in conjunction with the DECKBUILD run-time environment, which supports both interactive and batch mode operation [4]. TONYPLOT supplies scientific visualization capabilities [5].

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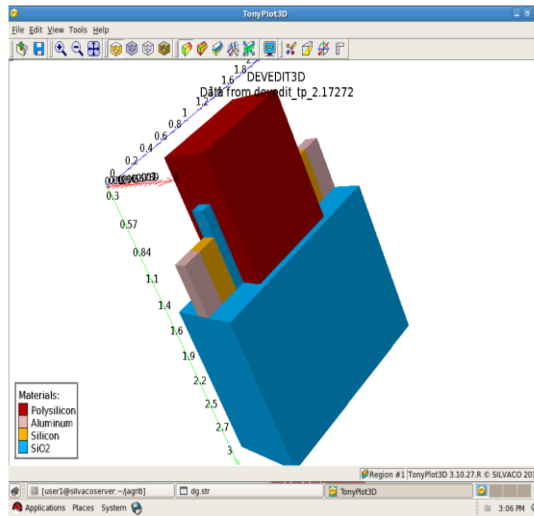

Figure 2 3D view of finfet

Silicon-On-Insulator transistors are fabricated in a small layer of silicon, located on the top of a silicon dioxide layer called buried oxide. This oxide layer provides full dielectric isolation of the transistor & thus most of the parasitic effects present in bulk silicon transistors are eliminated [7].

SIMULATION RESULTS

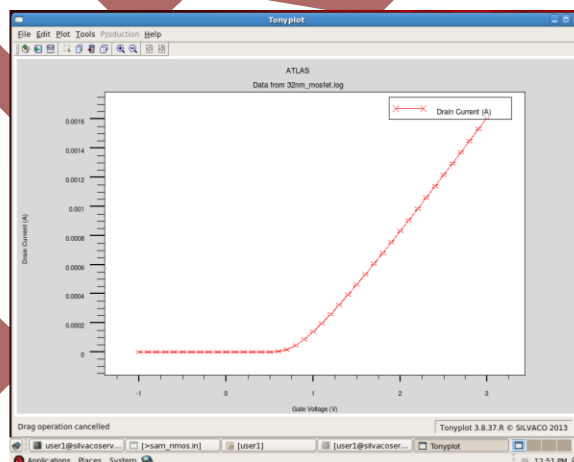

Figure 3 Transfer Characteristics of n-MOSFET

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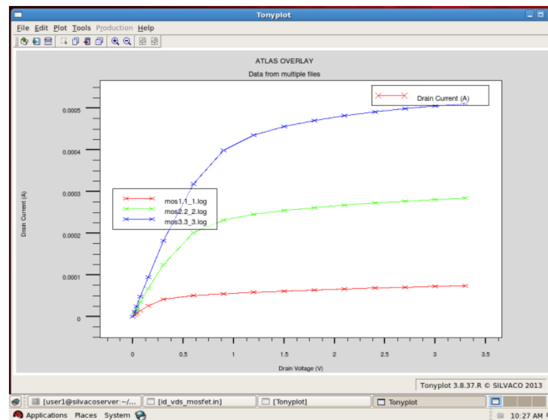

Figure 4 ID-VDS Characteristics of n-MOSFET

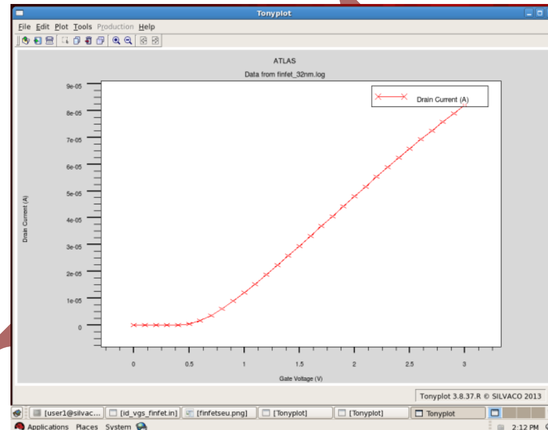

Figure 5 ID-VGS Characteristics of 32nm FINFET

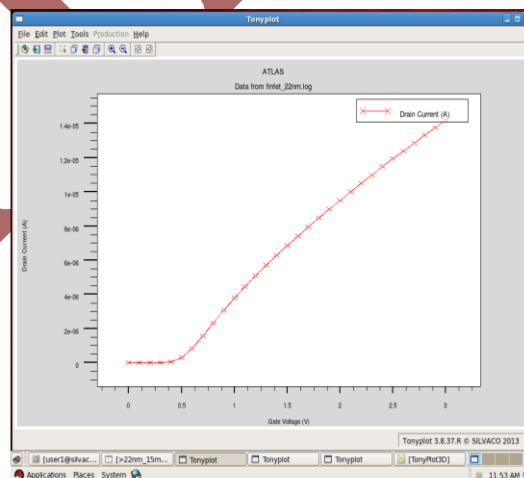

Figure 6 ID-VGS Characteristics of 22nm FINFET

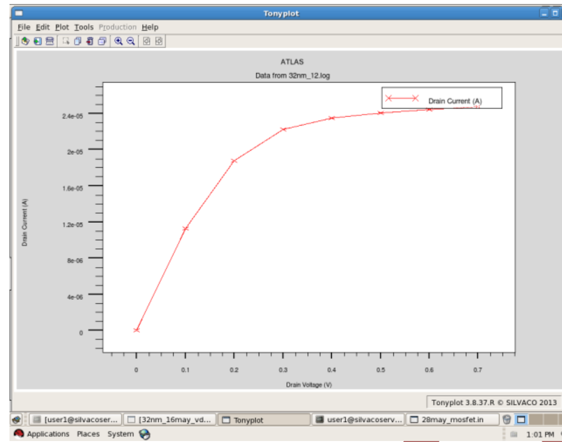

Figure 7 ID-VDS Characteristics of 32nm FINFET

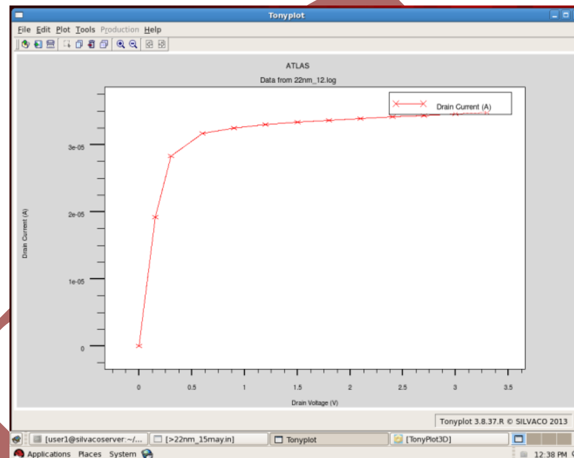

Figure 8 ID-VDS Characteristics of 22nm FINFET

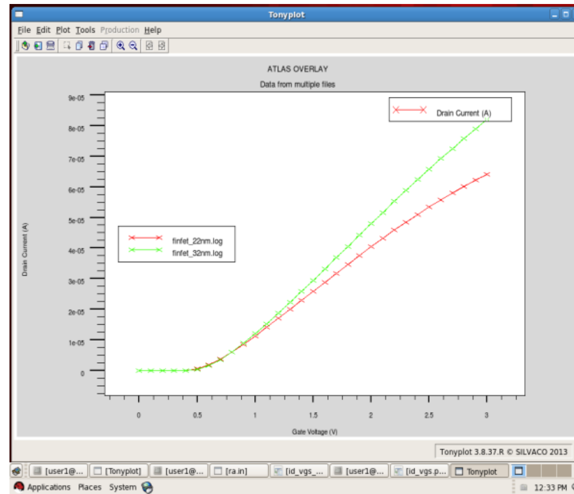

Figure 9 Overlay of 32nm & 22nm FINFET

Table 1 Parameters Comparison of MOSFET and FINFET at 32nm technology

Parameters	32nm	32nm
V_T	0.474764 V	0.202234V
Nidsmax	3.48439e-05	0.00761081
Sat Slope	6.96882e-07	0.00106298

Table 2 Parameters of FINFET at 22nm Technology

Parameters	22nm
V_T	0.122356V
Nidsmax	0.000510532
sat slope	1.87691e-05

CONCLUSION

Using SILVACO Tool simulation of MOSFET & Tri-gate FINFET based on SOI & plotted the corresponding results of simulation. The purpose of the work was to keep the scaling alive. Conventional MOSFET at 32nm technology is used. But FINFET based on SOI at the same technology is used which gives good results as compared with conventional MOSFET. FINFET

on SOI gives less threshold voltage as compared with MOSFET, hence FINFET require less power. It is also found that FINFET based on SOI posses the following key advantages over FINFET without SOI: Reduced short channel effects, excellent sub threshold slope, lower DIBL.

Simulation of FINFET at 22nm technology also performed. Overlay of FINFET at 32nm & 22nm technology also plotted & we can see that as the technology node becomes lower, threshold voltage reduced. Hence 22nm technology has good results compared with 32nm.

FUTURE SCOPE

This paper prospects that in future FinFET based on SOI can simulate at 20nm node & beyond. Power Consumption can be compared between two different scaling. This work can be implemented at the circuit level for calculating different factors.

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